VICTORIAN CURRICULUM AND ASSESSMENT AUTHORITY

Victorian Certificate of Education
2004

SUPERVISOR TO ATTACH PROCESSING LABEL HERE

STUDENT NUMBER

									Letter
Figures									
Words									

VCE VET ELECTRONICS

Written examination

Monday 1 November 2004

Reading time: 9.00 am to 9.15 am (15 minutes)
Writing time: 9.15 am to 10.45 am (1 hour 30 minutes)

QUESTION AND ANSWER BOOK

Structure of book

Section	*Number of questions*	*Number of questions to be answered*	*Number of marks*
1 – DC power supplies	5	5	32
2 – Analogue systems	5	5	31
3 – Digital electronics 1 and Digital systems	7	7	57
			Total 120

- Students are permitted to bring into the examination room: pens, pencils, highlighters, erasers, sharpeners, rulers, an approved graphics calculator (memory cleared) and/or one scientific calculator.
- Students are NOT permitted to bring into the examination room: blank sheets of paper and/or white out liquid/tape.

Materials supplied
- Question and answer book of 23 pages including a formula sheet for Sections 1, 2 and 3 on page 23.

Instructions
- Write your **student number** in the space provided above on this page.
- Answer **all** questions in the spaces provided in this book.
- **Note:** There are no separate items for Mathematics for Electronics 2. Understanding of mathematics has been incorporated into the questions in Sections 1–3.
- State all formulas and calculations.
- All units must be specified in the answers.
- All written responses must be in English.

Students are NOT permitted to bring mobile phones and/or any other electronic communication devices into the examination room.

SECTION 1 – DC power supplies

Question 1

The block diagram below in Figure 1 represents a linear DC power supply.

The four separate stages are represented by the blocks A, B, C and D.

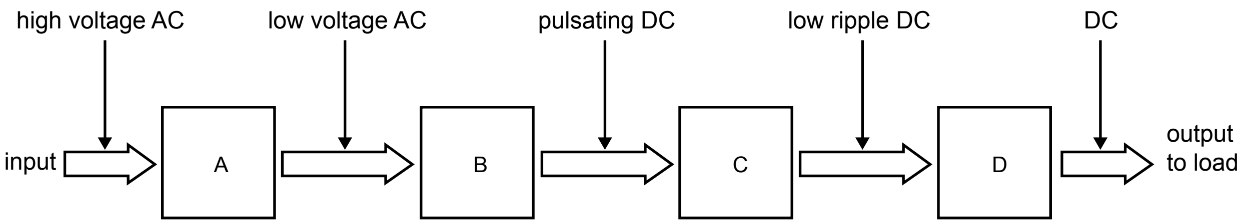


Figure 1

a. Which stage, A, B, C or D, is the filter stage?

1 mark

b. When functioning correctly the DC output stage should provide

A. a constant DC voltage level when the load is variable.

B. a constant DC current level at selected output voltages.

C. a variable DC voltage with a large AC ripple voltage.

D. a large ripple voltage when providing low output currents.

1 mark

Question 2

A simple rectifier circuit is shown below in Figure 2.

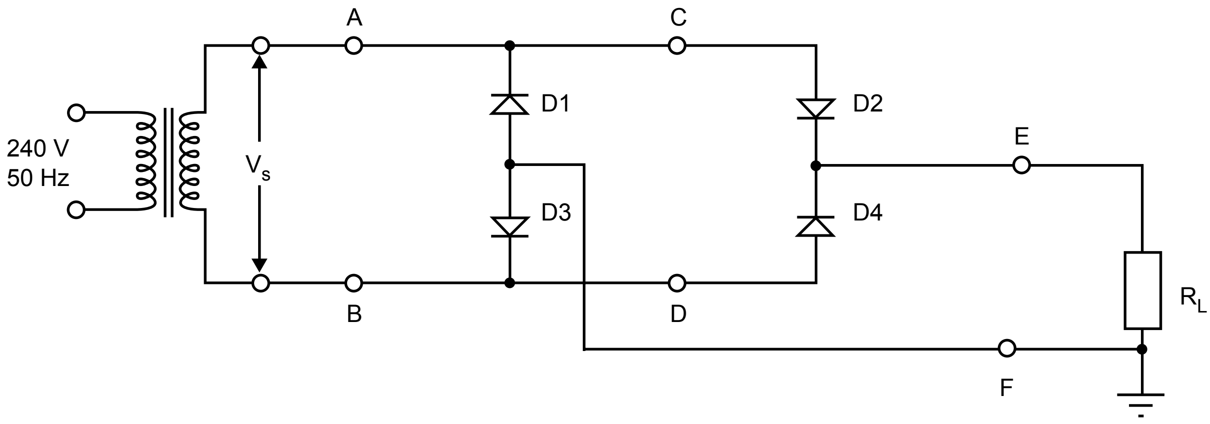


Figure 2

The circuit has the following parameters.

primary voltage, V_p = 240 V, 50 Hz
secondary voltage, V_s = 12 V, 50 Hz
load resistance, R_L = 1 kΩ
voltage drop for each diode, V_{drop} = 1 V

In questions where calculations are required, state the formula used and show substitution and correct units in the answer.

a. What is the name given to the configuration of the four diodes used in this circuit?

1 mark

b. What will be the ripple frequency at the load?

1 mark

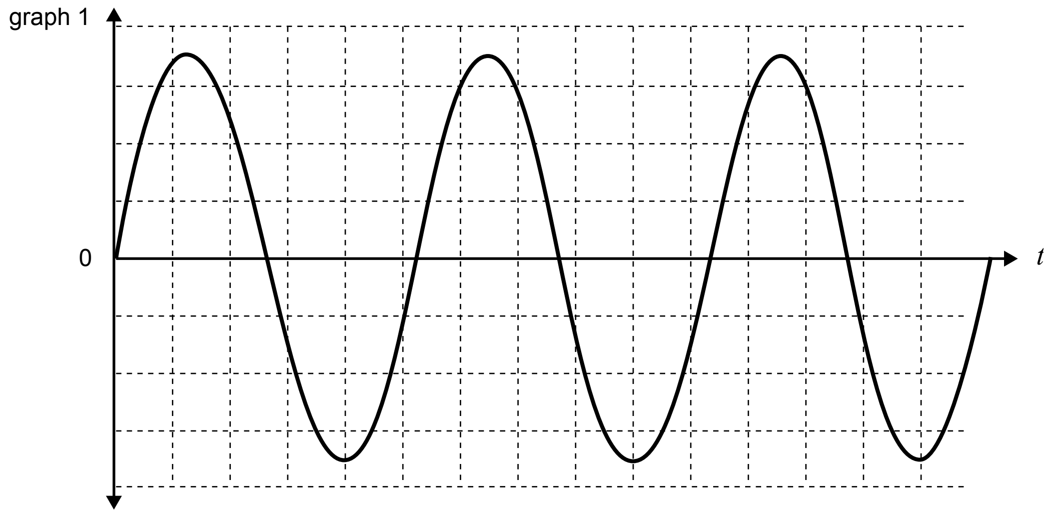
c. Calculate the peak level voltage across the load.

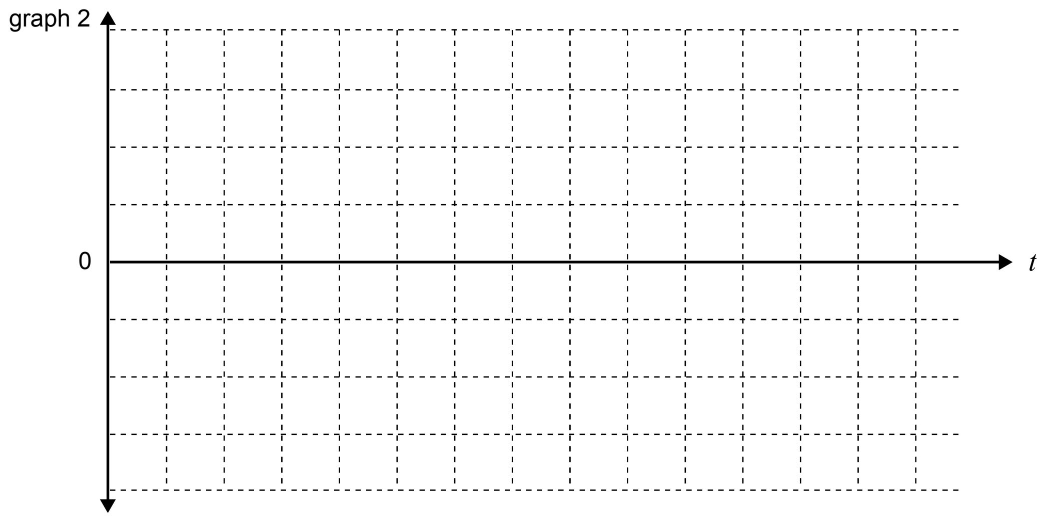
3 marks

d. Calculate the peak current through a conducting diode.

3 marks

Graph 1 represents the AC voltage at the secondary of the transformer, as would be seen in Figure 2 at nodes A and B.





e. On graph 2 draw the voltage waveform at node E with respect to Ground.

2 marks

f. State the number of diodes that conduct during each half cycle of rectification.

1 mark

Refer to Figure 2 on page 3 to answer parts **g.**, ***h.*** *and* ***i.***

A short circuit fault occurs across diode D1.

g. Explain the possible effects on the transformer.

2 marks

h. Suggest an additional component that could be used to protect the transformer against the short circuit fault condition for diode D1.

1 mark

A capacitor can be added to the circuit to produce an unregulated DC voltage at the load.

i. Where could the capacitor be placed?

A. between nodes A – B

B. between nodes C – D

C. between nodes E – F

D. It would not be placed in this part of the circuit at all.

1 mark

Use the following information to answer Questions ***3a.*** *and* ***3b.***

LM309 data sheet

National Semiconductor

January 1995

LM109/LM309 5-Volt Regulator

LM109/LM309 5-Volt Regulator

General Description

The LM109 series are complete 5V regulators fabricated on a single silicon chip. They are designed for local regulation on digital logic cards, eliminating the distribution problems association with single-point regulation. The devices are available in two standard transistor packages. In the solid-kovar TO-5 header, it can deliver output currents in excess of 200 mA, if adequate heat sinking is provided. With the TO-3 power package, the available output current is greater than 1A.

The regulators are essentially blowout proof. Current limiting is included to limit the peak output current to a safe value. In addition, thermal shutdown is provided to keep the IC from overheating. If internal dissipation becomes too great, the regulator will shut down to prevent excessive heating.

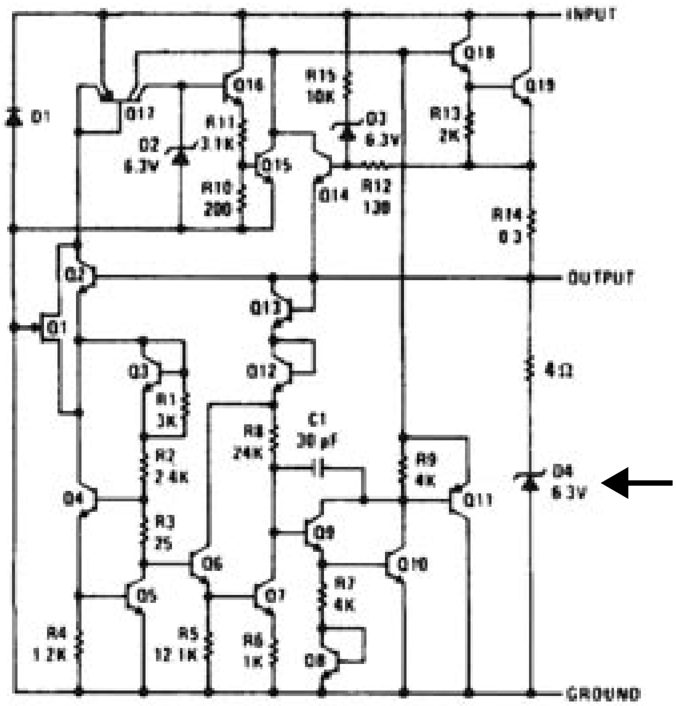
Considerable effort was expended to make these devices easy to use and to minimize the number of external components. It is not necessary to bypass the output, although this does improve transient response somewhat. Input bypassing is needed, however, if the regulator is located very far from the filter capacitor of the power supply. Stability is also achieved by methods that provide very good rejection of load or line transients as are usually seen with TTL logic.

Although designed primarily as a fixed-voltage regulator, the output of the LM109 series can be set to voltages above 5V, as shown. It is also possible to use the circuits as the control element in precision regulators, taking advantage of the good current-handling capability and the thermal overload protection.

Features

- Specified to be compatible, worst case, with TTL and DTL
- Output current in excess of 1A
- Internal thermal overload protection
- No external components required

Schematic Diagram



TL/H/7136–1

Question 3

A linear power supply using the LM309 regulator is shown in Figure 3.

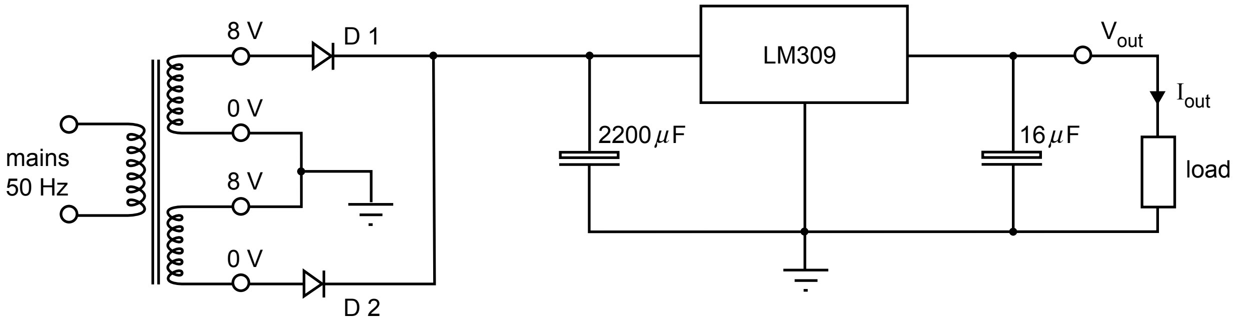


Figure 3

In questions where calculations are required, state the formula used and show substitution and correct units in the answer.

Refer to the LM309 data sheet on page 6 to answer parts ***a.*** *and* ***b.***

a. Determine the output voltage across the load.

1 mark

b. Name the type of component identified as D4 on the data sheet (schematic diagram).

1 mark

c. Refer to Figure 3.
Calculate the peak level of voltage across the 2200 μF capacitor in Figure 3.
(Assume ideal diodes.)

2 marks

The voltage regulator was initially designed for low levels of output current.

d. Briefly explain how a heat sink on the LM309 can increase the available maximum current output in the load.

2 marks

Question 4

Switch mode power supplies (SMPS) are increasingly being used to provide DC power for electronic items.
Name one electronic item that uses a SMPS to provide DC power.

1 mark

Question 5

A DC power supply, designed for a simple analogue application, is shown in Figure 4.
The circuit has the following parameters.

Average level of voltage across the 1000 μF capacitor = 10.8 V
Output current, I_{out} = 200 mA
Output voltage, V_{out} = 6 V

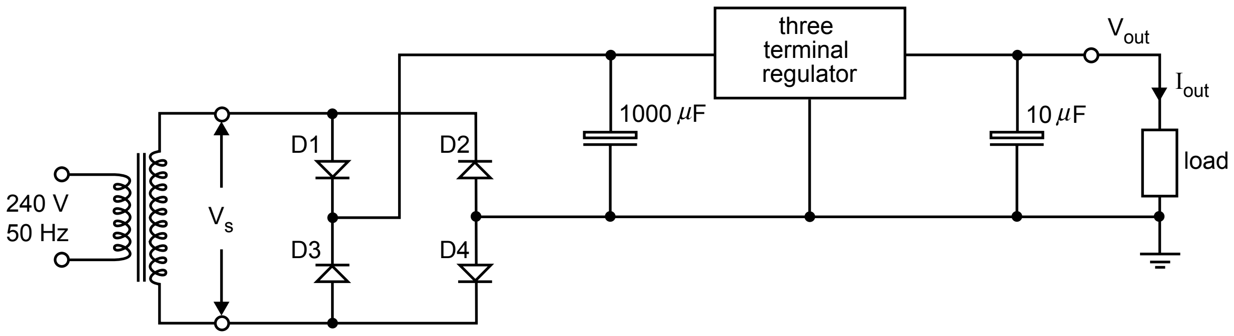


Figure 4

In questions where calculations are required, state the formula used and show substitution and correct units in the answer.

a. Calculate the power used by the load.

3 marks

b. Calculate the power dissipated by the three terminal regulator.

3 marks

A low value capacitor, 0.1 μF, is often placed at the input to the three terminal regulator when the 1000 μF capacitor is several centimetres away from the regulator.

c. Briefly explain why this low value capacitor is often used.

2 marks

Total 32 marks

END OF SECTION 1

SECTION 2 – Analogue systems

Below is a block diagram of a radio receiver.

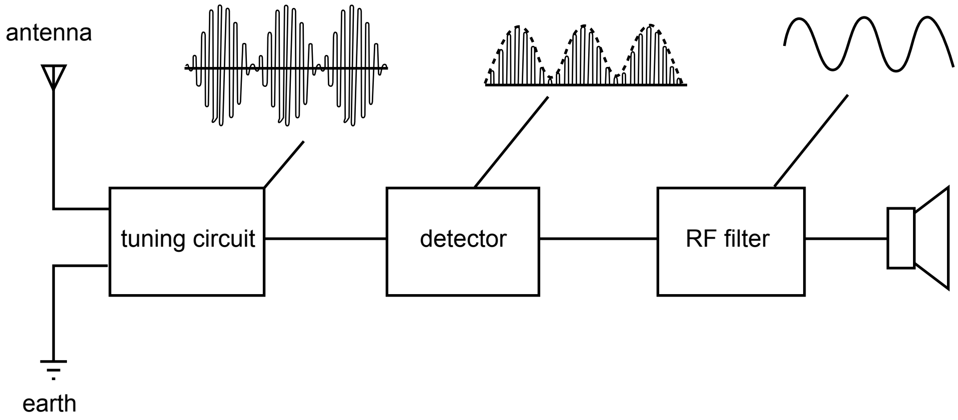


Figure 5

Question 1

a. What type of RF modulation is being received?

1 mark

b. What do the letters RF stand for?

1 mark

c. Briefly describe a function of the tuning circuit.

2 marks

d. A function of the detector section is to

A. maintain the volume level.
B. recover the original audio.
C. detect when the signal fades.
D. amplify the waveform.

1 mark

e. A function of the RF filter is to

A. pass only RF.
B. reduce signal fade.
C. pass only audio signals.
D. increase receiver volume levels.

1 mark

Question 2

A double-sided PCB design using CAD PCB design software is shown below in Figure 6.

The PCB shows two distinct areas, Section A and Section B.

Section A: An area on one side of the PCB where there is a large area of grounded copper.

Section B: This is where the 240 V AC power inputs are, shown by wide, well spaced tracks.

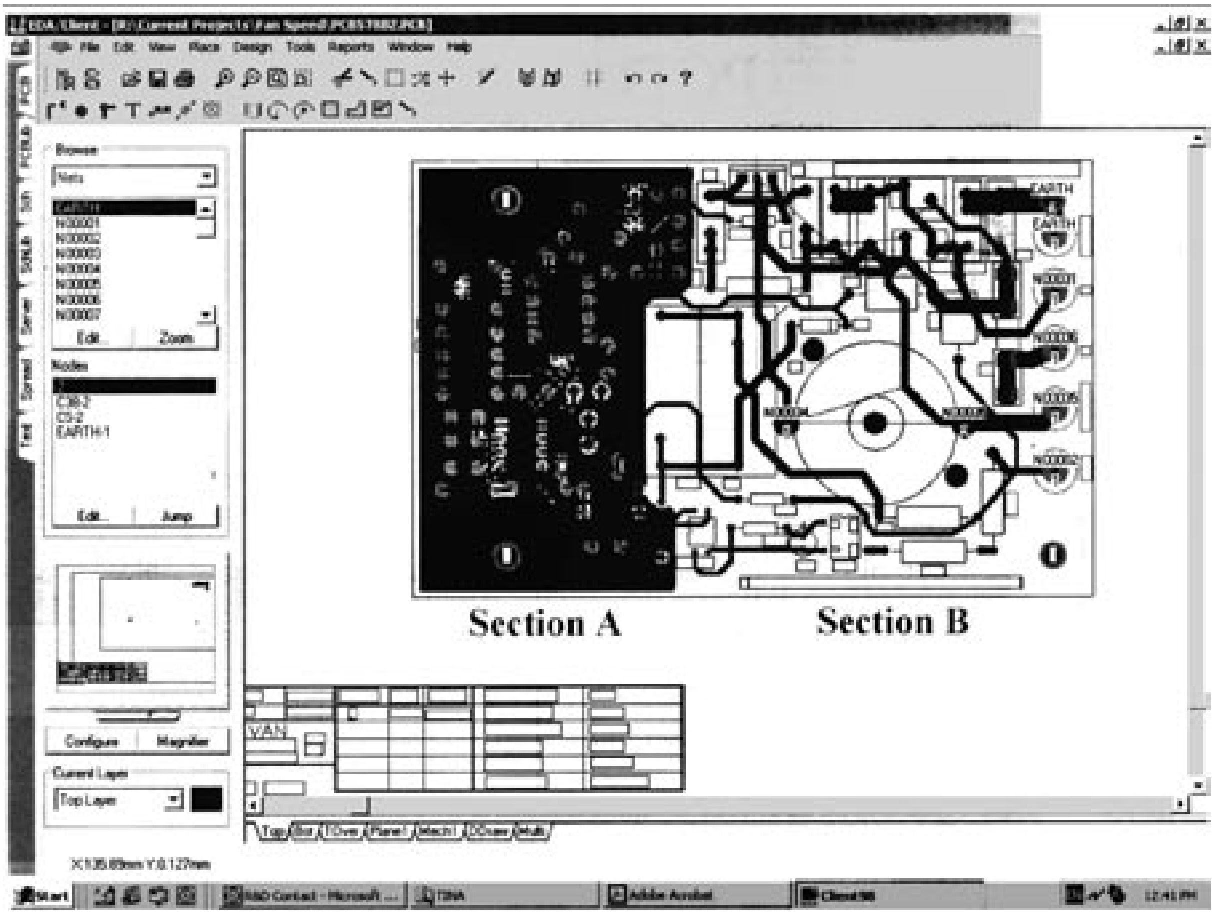


Figure 6

a. **i.** What do the letters CAD stand for?

____

ii. Name one CAD software program.

____

1 + 1 = 2 marks

In **Section A** of the PCB, there is a large area of 'grounded copper' on one side.

b. What general function does it perform?

1 mark

In **Section B** of the PCB, the circuit board has wide tracks which are well spaced apart.

c. What are the reasons for the wide tracks and spacing?

wide tracks

spacing

2 marks

Question 3

Transducer devices are used to convert one form of energy into another form.

Place a tick beside the items that are commonly used as transducers.

LED	
Disc capacitor	
BC548 transistor	
Thermocouple	

6 volt lamp	
3 volt solar cell	
Link wire	
LM741C (Op Amp)	

4 marks

Question 4

A dual LED flashing circuit is shown below in Figure 7. Refer to this circuit to answer the questions which follow.

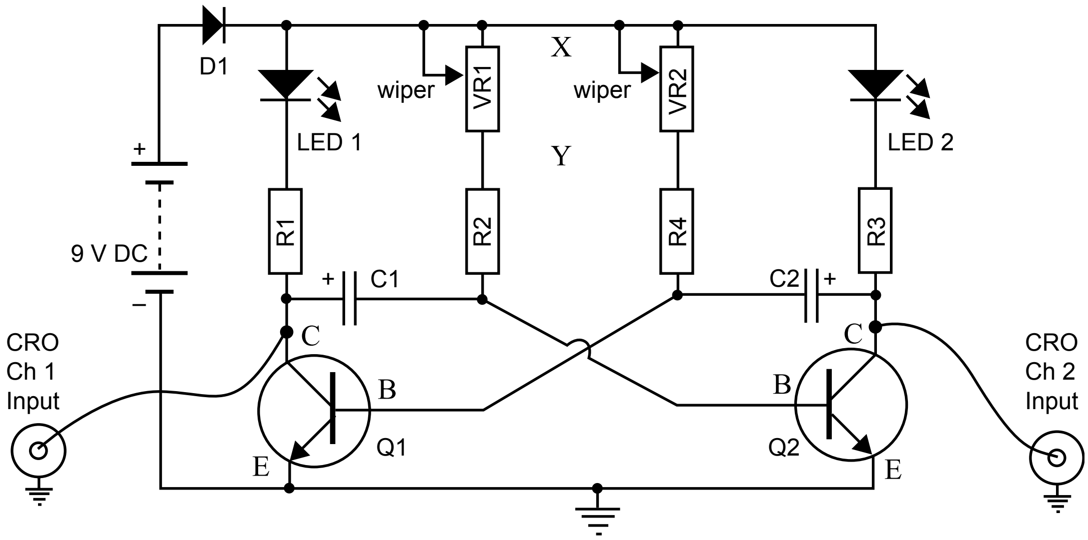


Figure 7

C1 is listed as a 10 μF capacitor.

a. What specific type of capacitor is appropriate for this application?

1 mark

b. **i.** What is the function of D1 in this circuit?

ii. How does it perform this function?

1 + 1 = 2 marks

c. If the circuit was functioning normally and D1 was suddenly shorted out, what effect would this have on the functioning of the circuit?

1 mark

d. What are components VR1 and VR2 commonly called?

1 mark

e. If the frequency of the flashing was too fast, which direction would the wipers on VR1 and VR2 be moved to slow the flashing?

A. The wipers would be moved up towards X.

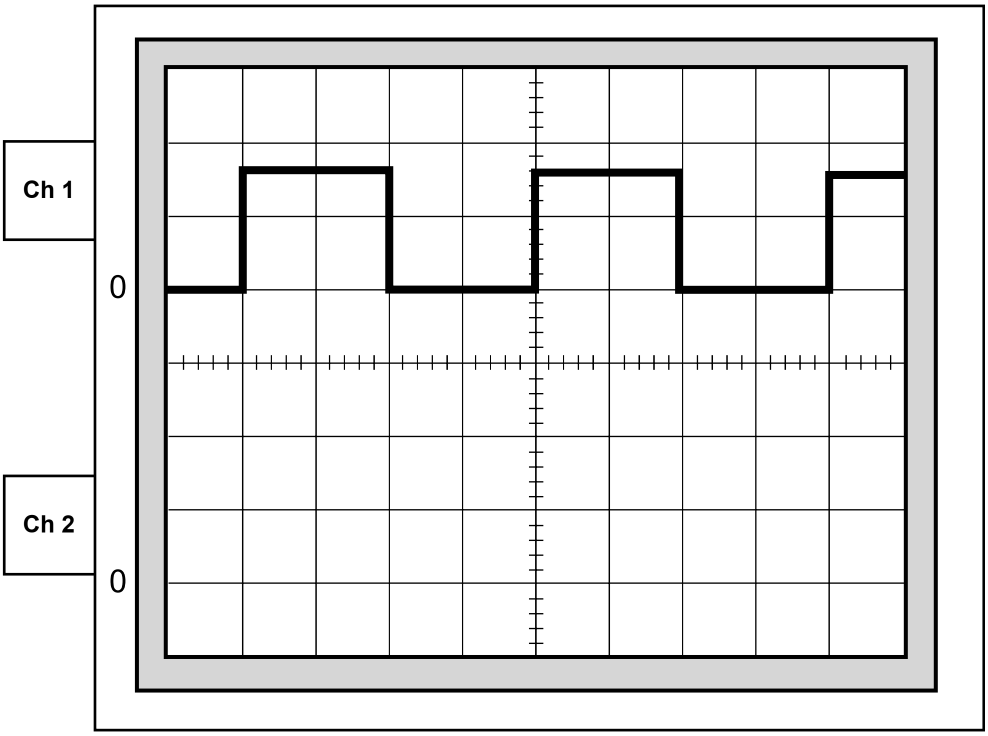
B. The wipers would be moved down towards Y.

C. It would not matter where the wipers were moved, the frequency is set.

1 mark

Both LEDs in this circuit in Figure 7 are flashing at the same frequency.

The following waveform was observed on a Cathode Ray Oscilloscope (CRO) when the Ch 1 probes were connected to the collector of Q1 and ground (0 volts).



- Time base set on 50 ms per cm
- Voltage set on 5 volts per cm

f. Given the provided CRO settings

i. determine the frequency of the signal on Ch 1.

ii. determine the peak voltage of the signal on Ch 1.

2 + 1 = 3 marks

g. Ch 2 probes were connected to the collector of Q2 and Ground. Draw in the expected Ch 2 waveform on the lower half of the screen.

Assume the CRO settings for the Ch 2 input are the same as for Ch 1, as given above.

2 marks

Use the following information to answer Question 5.

LM555 data sheet

LM 555 Data Sheet

Absolute Maximum Ratings

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage +18V

Power Dissipation (Note 1)
- LM555H, LM555CH 760 mW
- LM555, LM555CN 1180 mW

Operating Temperature Ranges
- LM555C 0°C to +70°C
- LM555 −55°C to +125°C

Storage Temperature Range −65°C to +150°C

Soldering Information
- Dual-In-Line Package
  - Soldering (10 Seconds) 260°C
- Small Outline Package
  - Vapor Phase (60 Seconds) 215°C
  - Infrared (15 Seconds) 220°C

See AN-450 "Surface Mounting Methods and Their Effect on Product Reliability" for other methods of soldering surface mount devices.

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless othewise specified)

Parameter	Conditions	Limits LM555 Min	LM555 Typ	LM555 Max	LM555C Min	LM555C Typ	LM555C Max	Units
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		10	12		10	15	mA
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature	R_A, R_B = 1k to 100 kΩ, C = 0.1 μF, (Note 3)		90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV

Question 5

A flashing LED circuit, as shown in Figure 8 below, can be made using a LM555 timer.

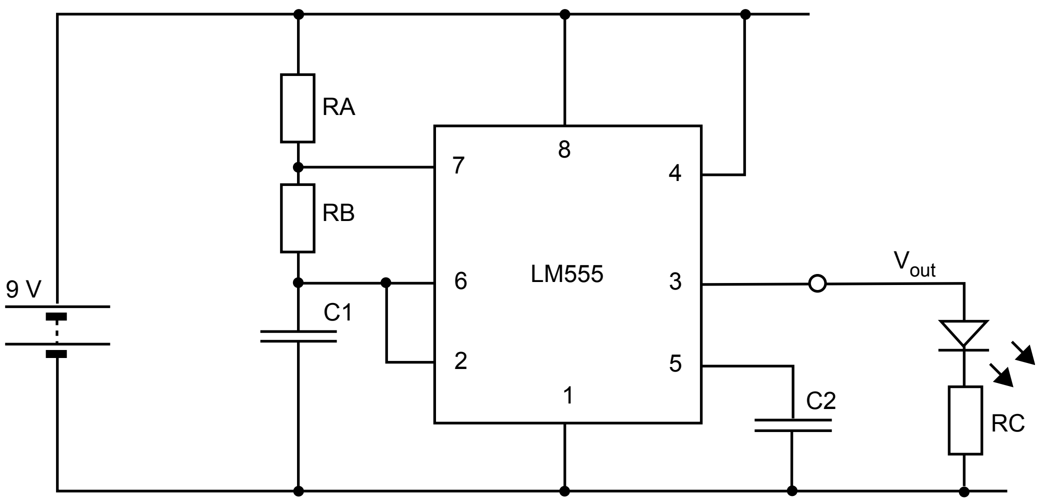


Figure 8

The frequency of oscillation is given by the equation

$$f = \frac{1 \cdot 44}{C1 \times (RA + 2\,RB)}$$

a. Calculate the oscillation frequency at V_{out} using the provided formula.

When: RA = 22 kΩ, RB = 22 kΩ and C1 = 22 μF

Formula, substitution and correct units must be shown.

3 marks

b. What would be the approximate peak-to-peak voltage at V_{out}?

1 mark

c. Refer to the data sheet on page 14 for a LM555.

What is the operating voltage range of the LM555?

1 mark

Total 31 marks

END OF SECTION 2
TURN OVER

SECTION 3 – Digital electronics 1 and Digital systems

CD4017B data sheet

National Semiconductor

March 1988

CD4017BM/CD4017BC Decade Counter/Divider with 10 Decoded Outputs
CD4022BM/CD4022BC Divide-by-8 Counter/Divider with 8 Decoded Outputs

General Description

The CD4017BM/CD4017BC is a 5-stage divide-by-10 Johnson counter with 10 decoded outputs and a carry out bit.

The CD4022BM/CD4022BC is a 4-stage divide-by-8 Johnson counter with 8 decoded outputs and a carry-out bit.

These counters are cleared to their zero count by a logical "1" on their reset line. These counters are advanced on the positive edge of the clock signal when the clock enable signal is in the logical "0" state.

The configuration of the CD4017BM/CD4017BC and CD4022BM/CD4022BC permits medium speed operation and assures a hazard free counting sequence. The 10/8 decoded outputs are normally in the logical "0" state and go to the logical "1" state only at their respective time slot. Each decoded output remains high for 1 full clock cycle. The carry-out signal completes a full cycle for every 10/8 clock input cycles and is used as a ripple carry signal to any succeeding stages.

Features

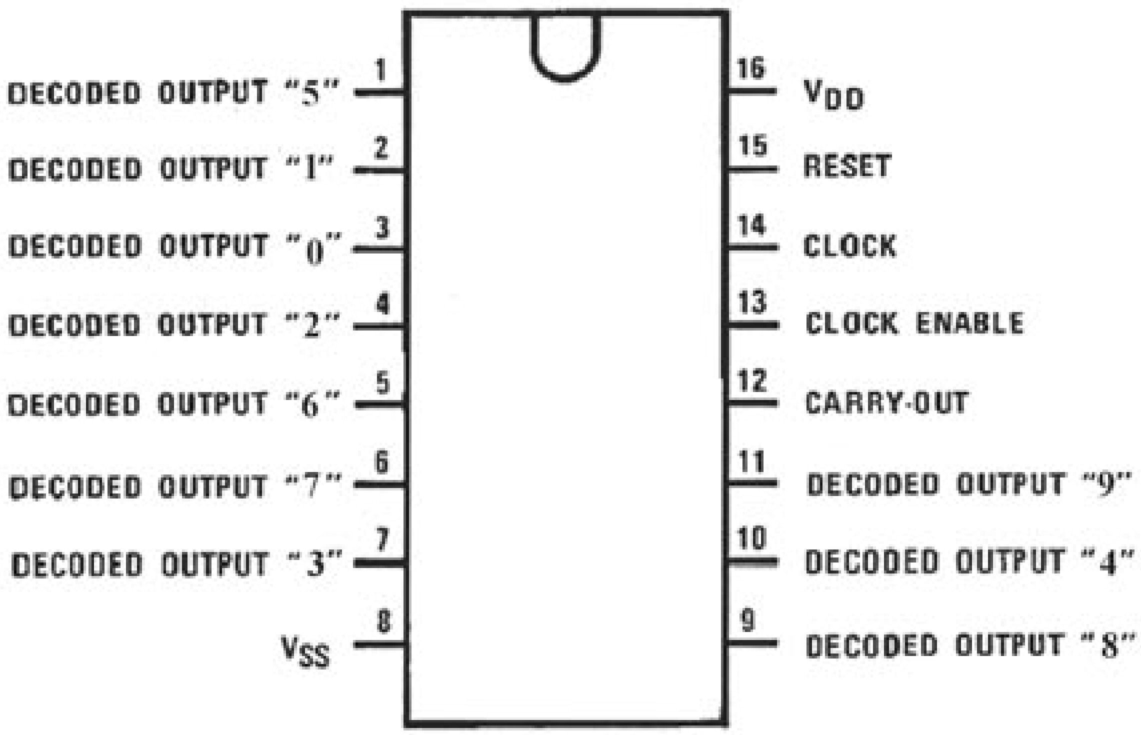
- Wide supply voltage range 3.0V to 15V
- High noise immunity 0.45 V_{DD} (typ.)
- Low power TTL compatibility Fan out of 2 driving 74L or 1 driving 74LS
- Medium speed operation 5.0 MHz (typ.) with 10V V_{DD}
- Low power 10 µW (typ.)
- Fully static operation

Applications

- Automotive
- Instrumentation
- Medical electronics
- Alarm systems
- Industrial electronics
- Remote metering

Connection Diagrams

Order Number CD4017B



Top View

RRD-B30M105/Printed in U. S. A.

CD4017BM/CD4017BC Decade Counter/Divider with 10 Decoded Outputs
CD4022BM/CD4022BC Divide-by-8 Counter/Divider with 8 Decoded Outputs

Question 1

Figure 9 below is an electronic dice circuit. This circuit utilises the LM555 timer IC, as a clock for the CD4017B IC.

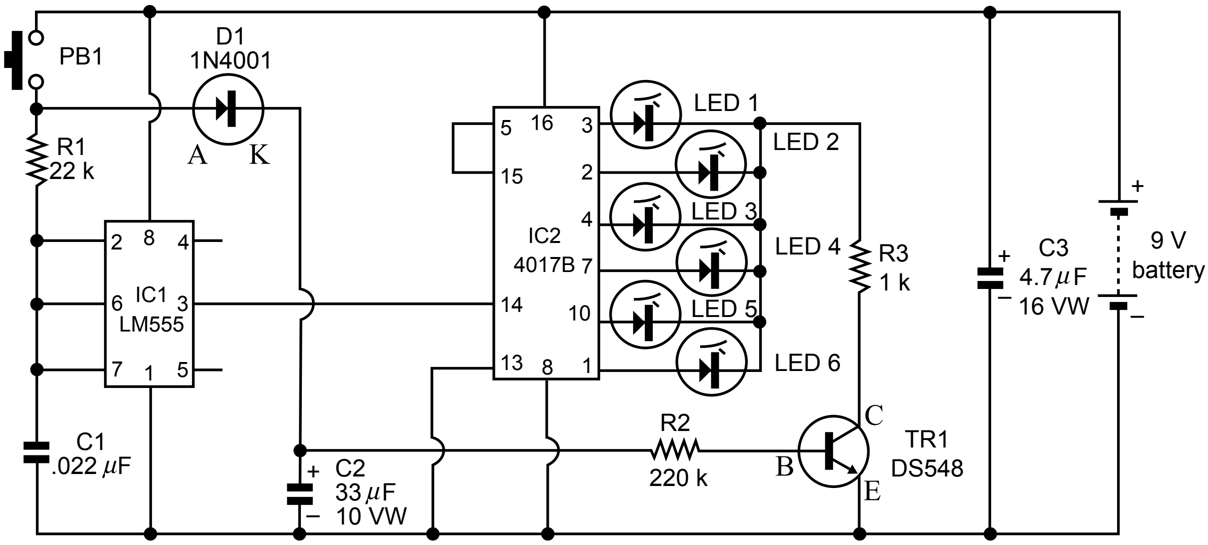


Figure 9

a. What two standard components could be changed in order to slow down the clock input?

____

____

2 marks

b. Refer to the data sheet for the CD4017B on page 16.

i. Which logic device family does the CD4017B belong to?

____

ii. What standard precautions would you take in handling this type of IC?

____

1 + 1 = 2 marks

A new game required the dice to count up to eight. Two more LEDs (LED 7 and 8) were added to the circuit to allow the circuit to do this.

c. Complete the table below for the pin CD4017B connections for LED 5, LED 6, LED 7 and LED 8.

CD4017B LED outputs							
LED 1	*LED 2*	*LED 3*	*LED 4*	LED 5	LED 6	LED 7	LED 8
Count 1. Decoded Output '0'	Count 2. Decoded Output '1'	Count 3. Decoded Output '2'	Count 4. Decoded Output '3'	Count 5. Decoded Output '4'	Count 6. Decoded Output '5'	Count 7. Decoded Output '6'	Count 8. Decoded Output '7'
Pin 3	Pin 2	Pin 4	Pin 7	**Pin** _____	**Pin** _____	**Pin** _____	**Pin** _____

2 marks

d. There is now a total of 8 LEDs in the display.

i. What **'Count'** would trigger the CD4017B to reset?

Connection changes need to be made to the circuit to allow the counter to reset.

ii. What existing pin connections on the IC would need to be removed?

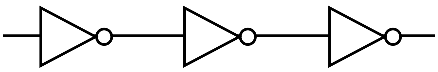
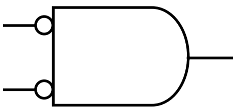
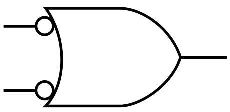
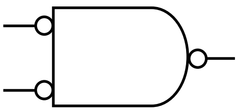
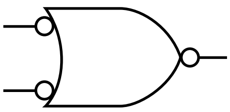
iii. What new connections on the IC would allow it to reset?

2 + 2 + 2 = 6 marks

Question 2

Draw the equivalent gate type for each gate combination below and state its correct name.

The simplified equivalent gates may be determined by using any suitable method; for example, De Morgan's laws.

combination gate	equivalent gate (simplified)	
symbol	symbol	name
		
		
		
		
		

10 marks

Question 3

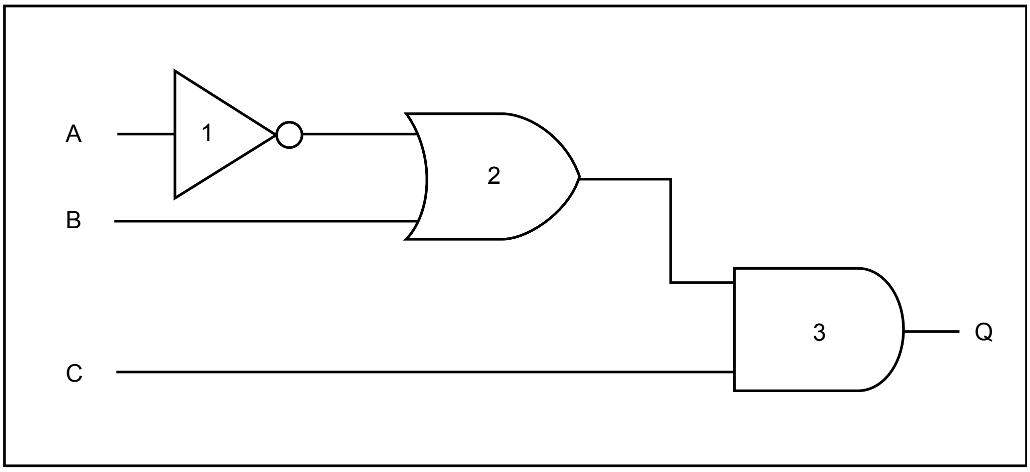


Figure 10

a. Identify the gate types in Figure 10.

gate number	gate type
gate 1	
gate 2	
gate 3	

3 marks

b. Complete the following truth table for the logic circuit in Figure 10 by

i. completing the Boolean expressions for gates 2 and 3

ii. completing the missing logic level outputs for gates 1, 2 and 3.

Inputs			Outputs		
			gate 1	gate 2	gate 3
C	B	A	$\overline{A}$	________	________ = Q
0	0	0	1	1	0
0	0	1		0	0
0	1	0			0
0	1	1			0
1	0	0		1	
1	0	1		0	
1	1	0			
1	1	1	0		

2 + 14 = 16 marks

Question 4

Complete the following number conversions.

a.

decimal	binary	BCD
1234		

2 marks

b.

hexadecimal	binary	decimal
ABC		

2 marks

Question 5

The ASCII code set is shown below.

Most significant hexadecimal digit

Least significant hexadecimal digit

	2	3	4	5	6	7
0	SP	0	@	P	`	p
1	!	1	A	Q	a	q
2	"	2	B	R	b	r
3	#	3	C	S	c	s
4	$	4	D	T	d	t
5	%	5	E	U	e	u
6	&	6	F	V	f	v
7	'	7	G	W	g	w
8	(	8	H	X	h	x
9	)	9	I	Y	i	y
A	*	:	J	Z	j	z
B	+	;	K	[	k	{
C	,	<	L	\	l	|
D	_	=	M	]	m	}
E	.	>	N	^	n	~
F	/	?	O	_	o	DEL

a. Using the table provided decode the hex ASCII code below.

ASCII HEX	**45**	**6C**	**65**	**63**	**74**	**72**	**6F**	**6E**	**69**	**63**
character										

2 marks

The ASCII HEX code is processed in the computer as a 7 bit binary number.

The first 3 numbers are shown below.

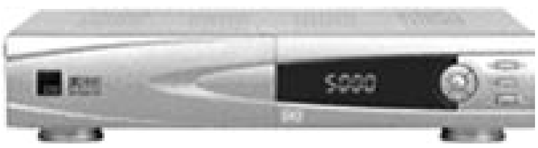
b. Covert the ASCII HEX to ASCII binary.

ASCII HEX	45	6C	65
ASCII Binary 7 bit			

3 marks

Question 6

'Set Top Boxes' (example below), which are connected to conventional analogue televisions, have recently been introduced.



Give a brief description of the basic function of the Set Top Box.

___

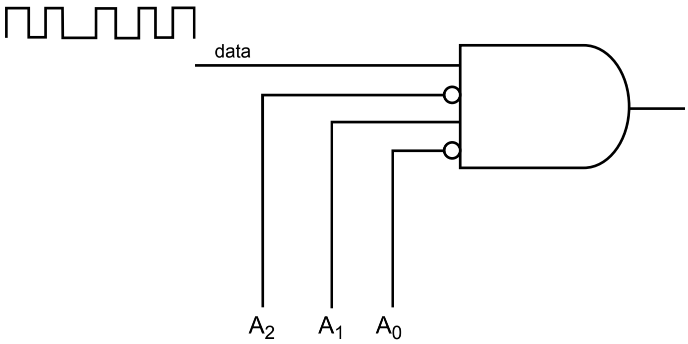
___

___

3 marks

Question 7

The gate shown below allows data to be transferred when input conditions are correctly set.



a. Complete the following sentence.

The little circle shown on the input, A_2, indicates that this input is an active ____________ input.

1 mark

b. Complete the table for inputs A_0, A_1 and A_2, indicating the logic level (H or L) which will allow data to be transferred via the gate.

inputs	logic level
A_2	
A_1	
A_0	

3 marks

Total 57 marks

END OF SECTION 3

Formulas

$V = I \times R$

$P = V \times I$

$V_{pk} = \sqrt{2} \times V_s$

$f = \dfrac{1}{T}$

$V_{reg} = V_{in} - V_{out}$

Other specific formulas are provided within the paper.

END OF QUESTION AND ANSWER BOOK